Docket No.: 60188-156 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Masahiro FUKUI, et al. :

Serial No.: : Group Art Unit:

Filed: March 01, 2002 : Examiner:

For: WIRING METHOD IN LAYOUT DESIGN OF SEMICONDUCTOR INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT AND FUNCTIONAL MACRO

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE CLAIMS:

Please amend the Claims as follows:

16. The semiconductor integrated circuit of Claim 13, wherein the width of the plurality of interconnection lines is 0.18 μm or less.

17. The semiconductor integrated circuit of Claim 13, wherein the plurality of interconnection lines are a plurality of address bus lines.